

Model Name : ZIWB0/ZIWB1/ZIWE0  
File Name :

# Compal Confidential

## ZIWB0/ZIWB1/ZIWE0 DIS M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

14PCB@  
DA1 PCB

Part Number	Description
DA60013Y010	REV1.0 M/B

15PCB@  
DA2 PCB

Part Number	Description
DA60013Y110	REV1.0 M/B

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

Device	Address
GPU	0x9E
Thermal	1001_101xb

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

43 level BOM table

43 Level	Description	BOM Structure

USOC1  
N2920@

S IC FH8065301616203 SR1SF B3 1.86G C38!  
Part Number = SA00007E860

USOC1  
N3520@

S IC FH8065301616103 SR1SE B3 2.17G C38!  
Part Number = SA00007E990

USOC1  
N2815@

S IC FH8065301619509 SR1SJ B3 1.86G C38!  
Part Number = SA00007EO50

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				Date: Tuesday, February 18, 2014	Rev 0.2 Sheet 3 of 47

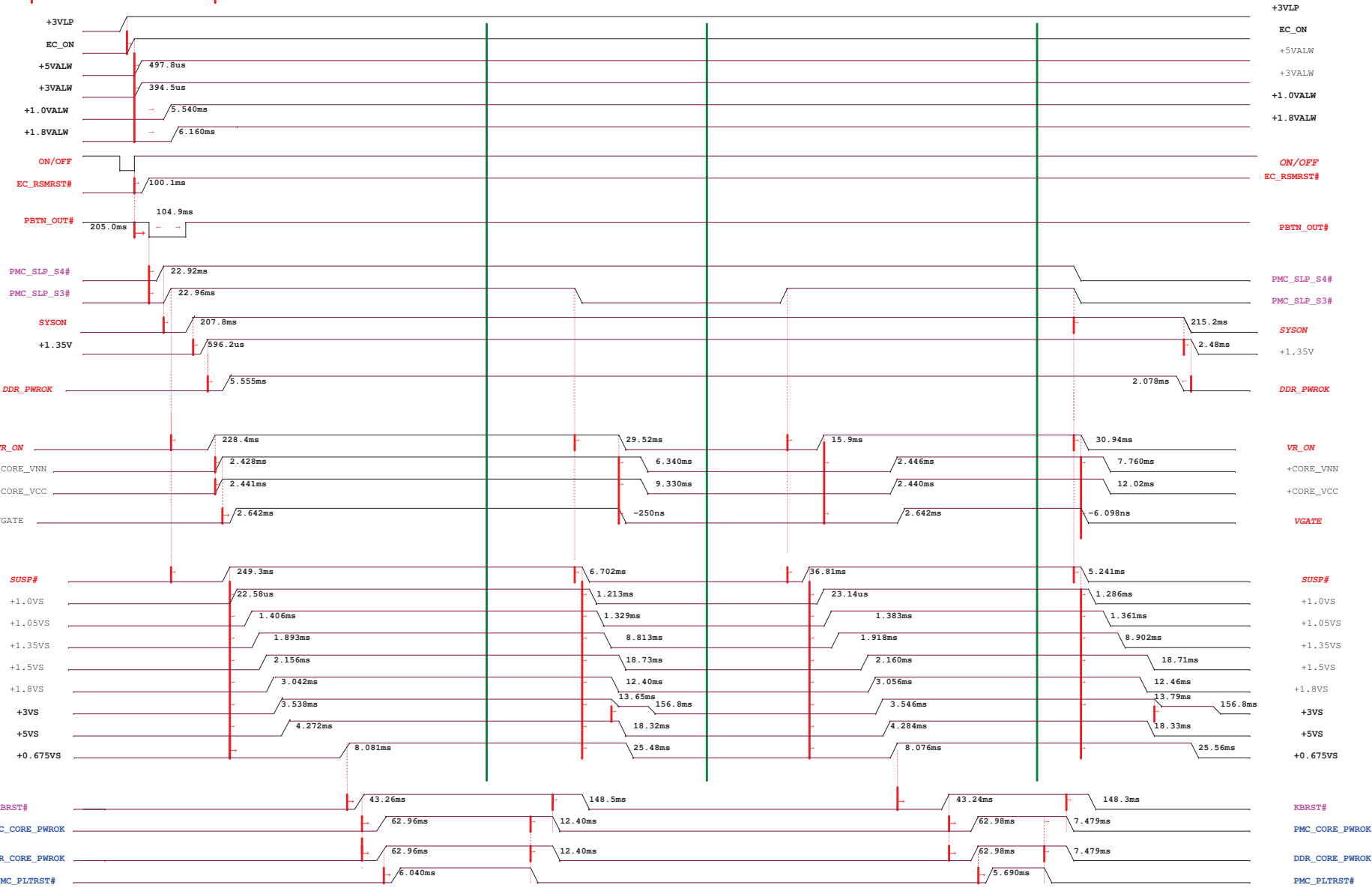
Power On

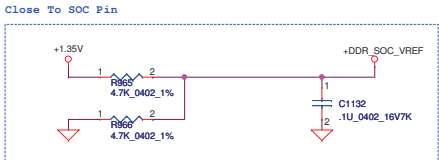
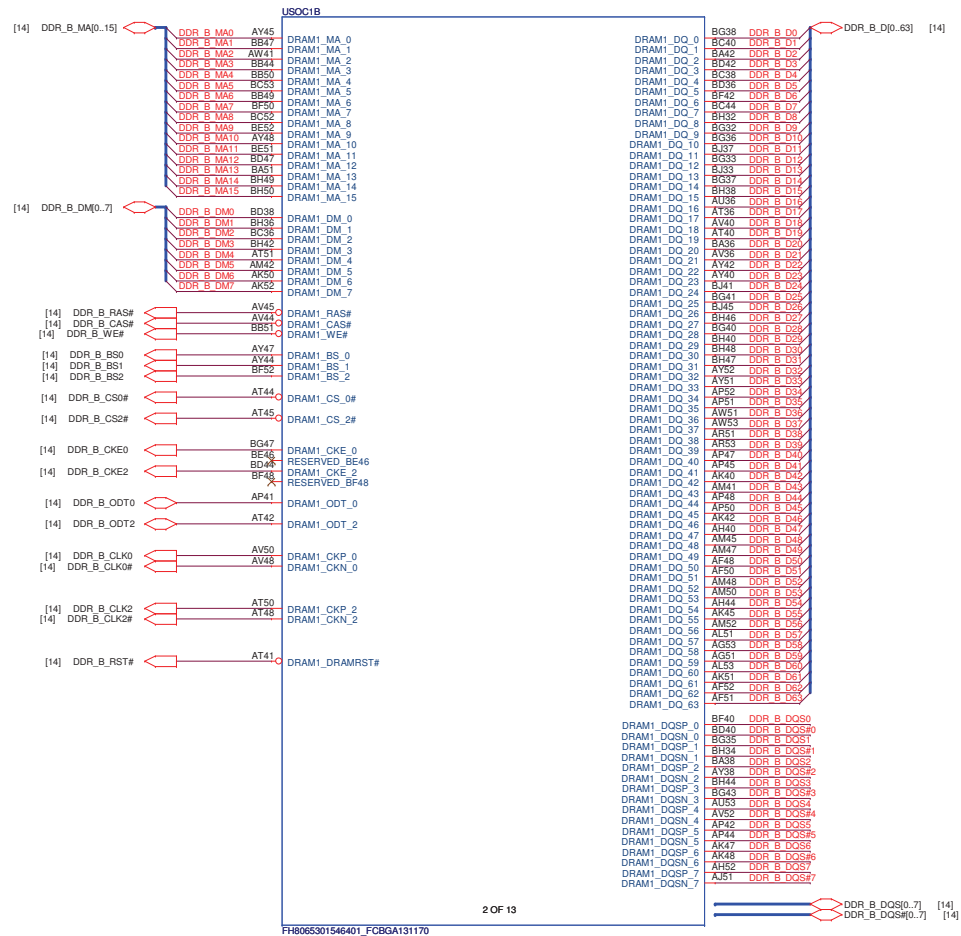
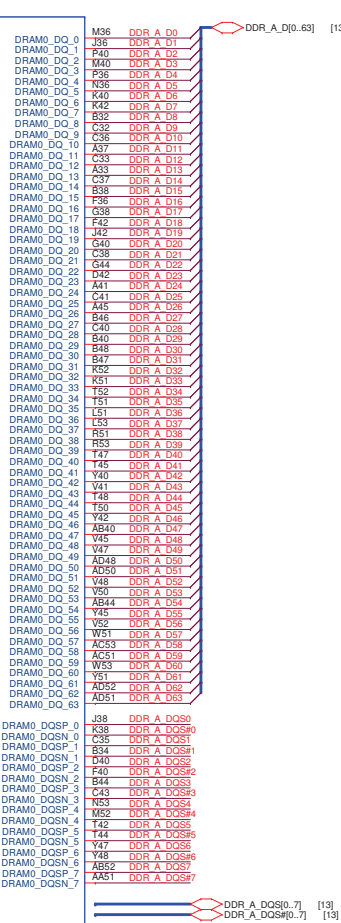
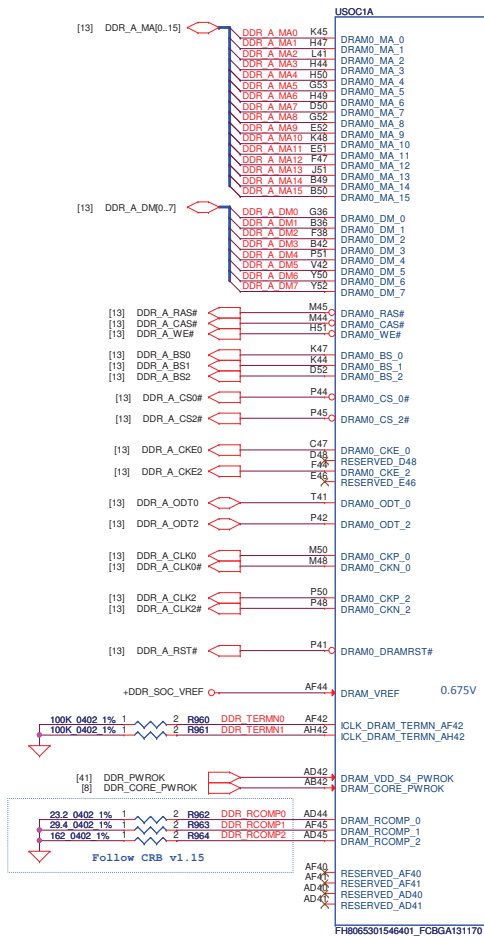
S3

S3 Resume

Power Off

Plug in



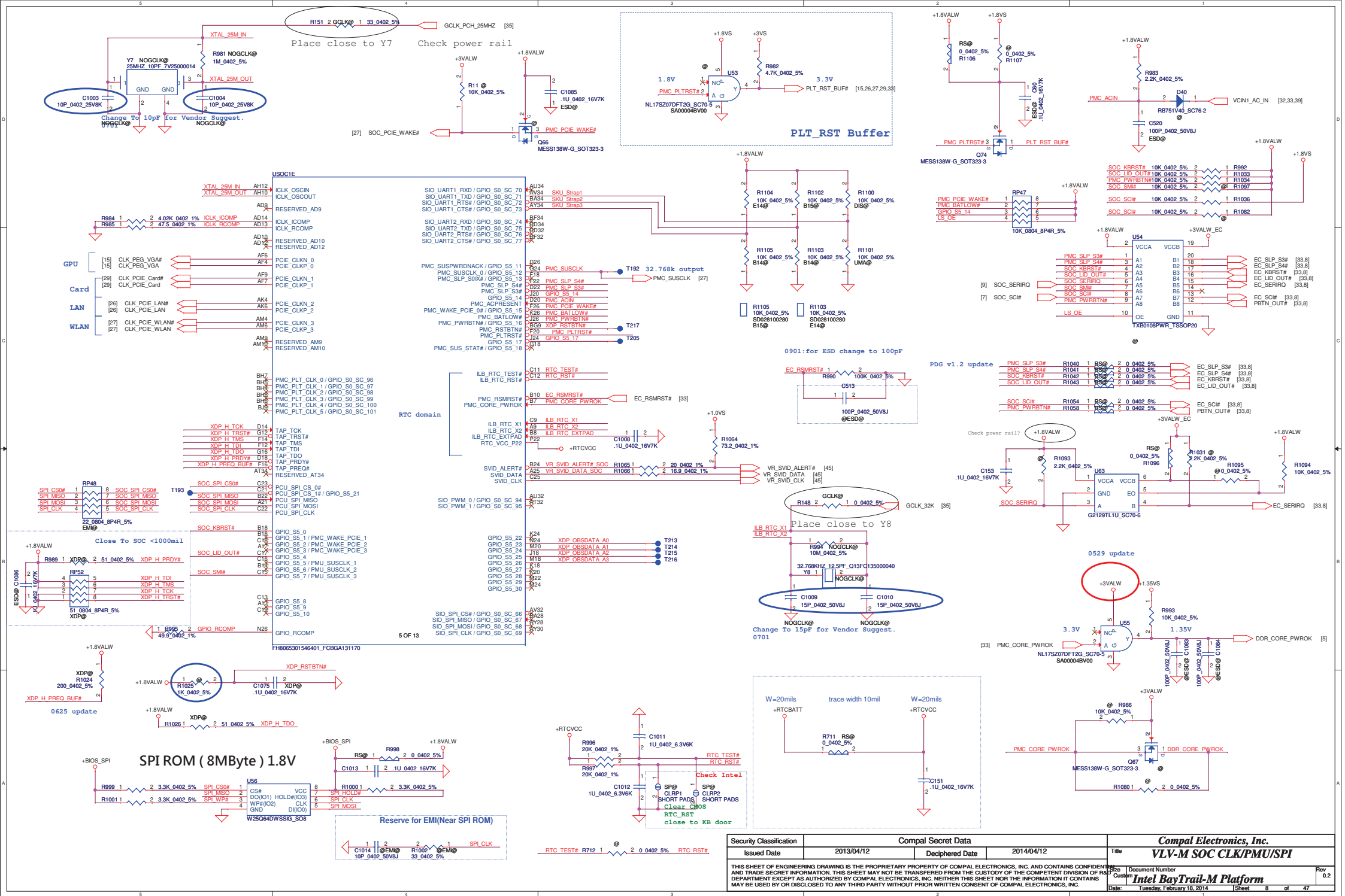


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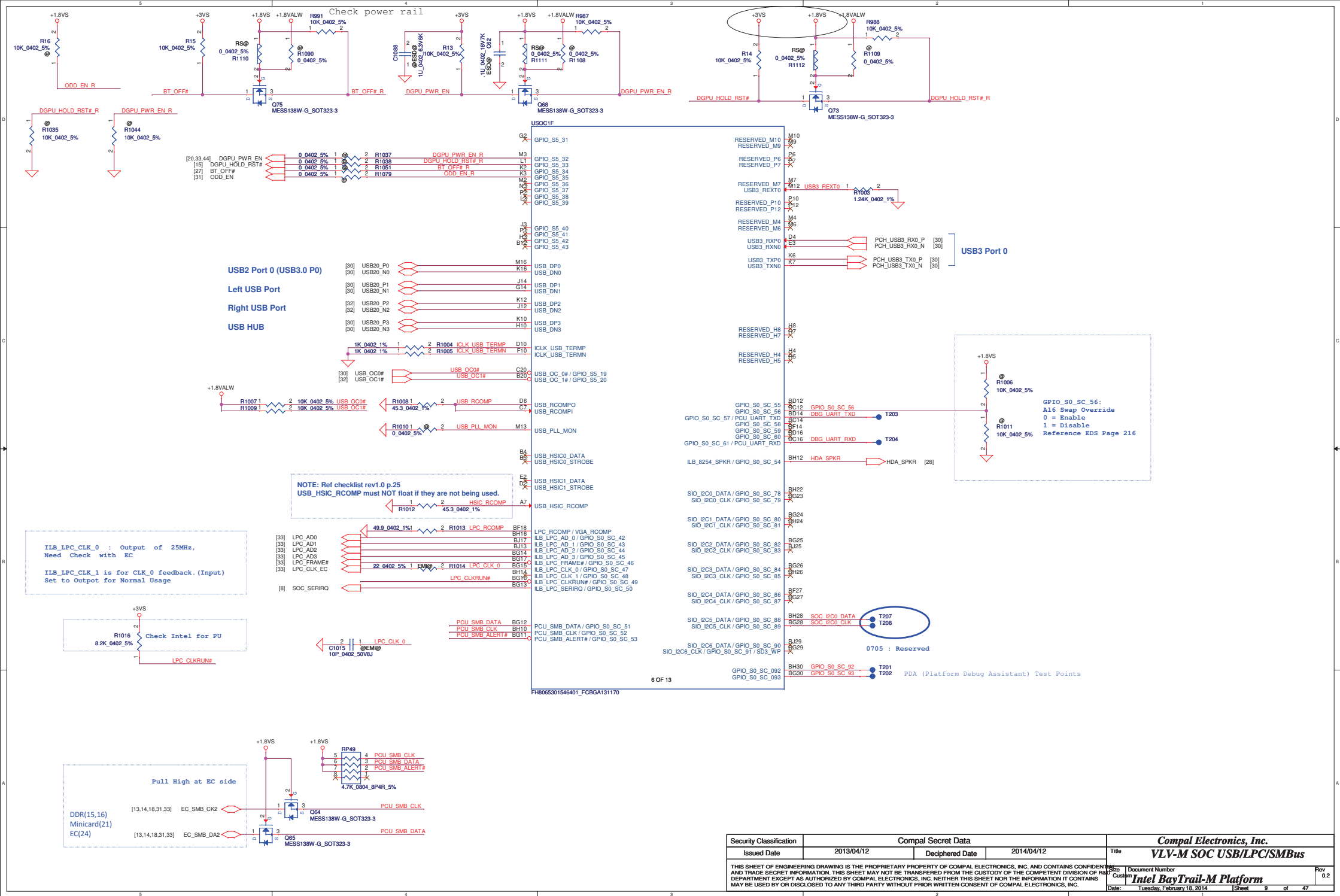




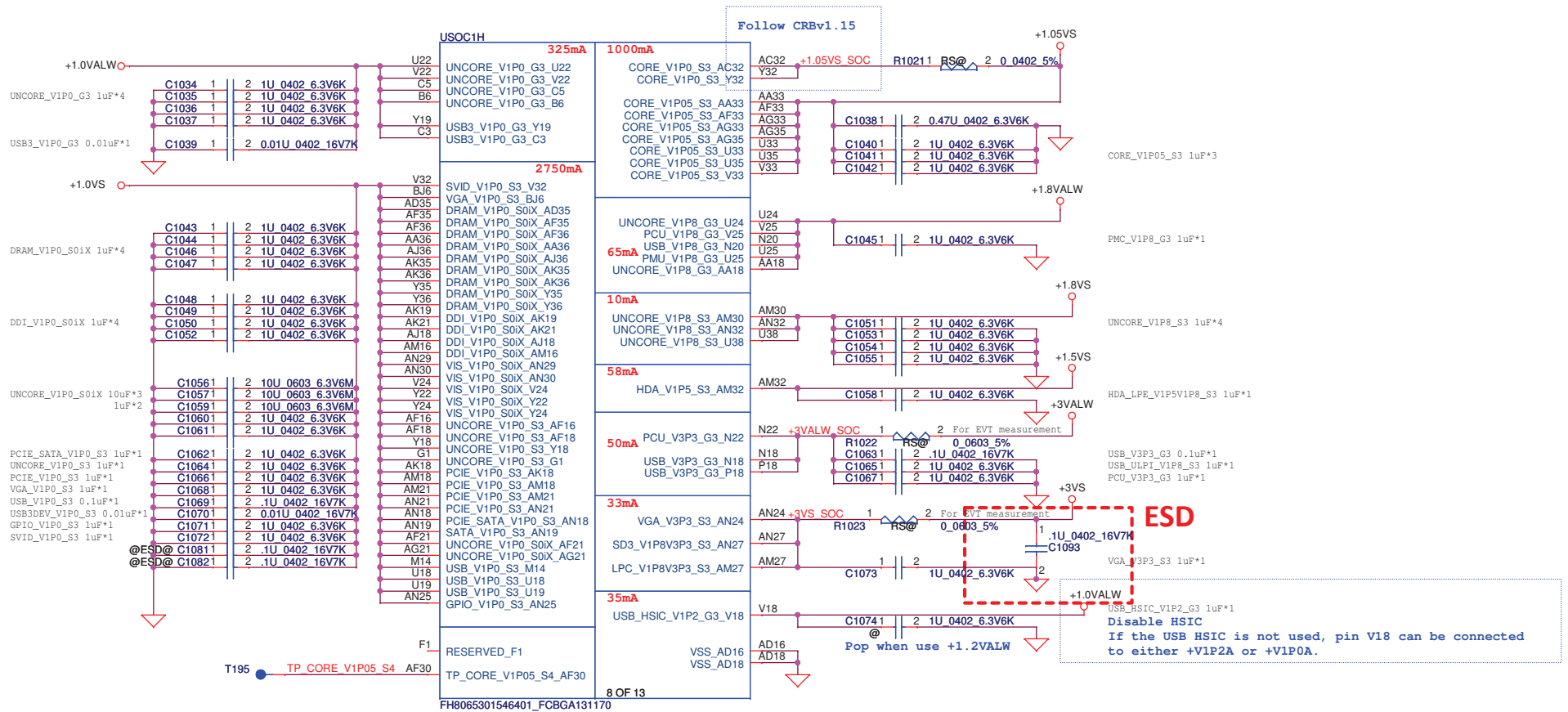




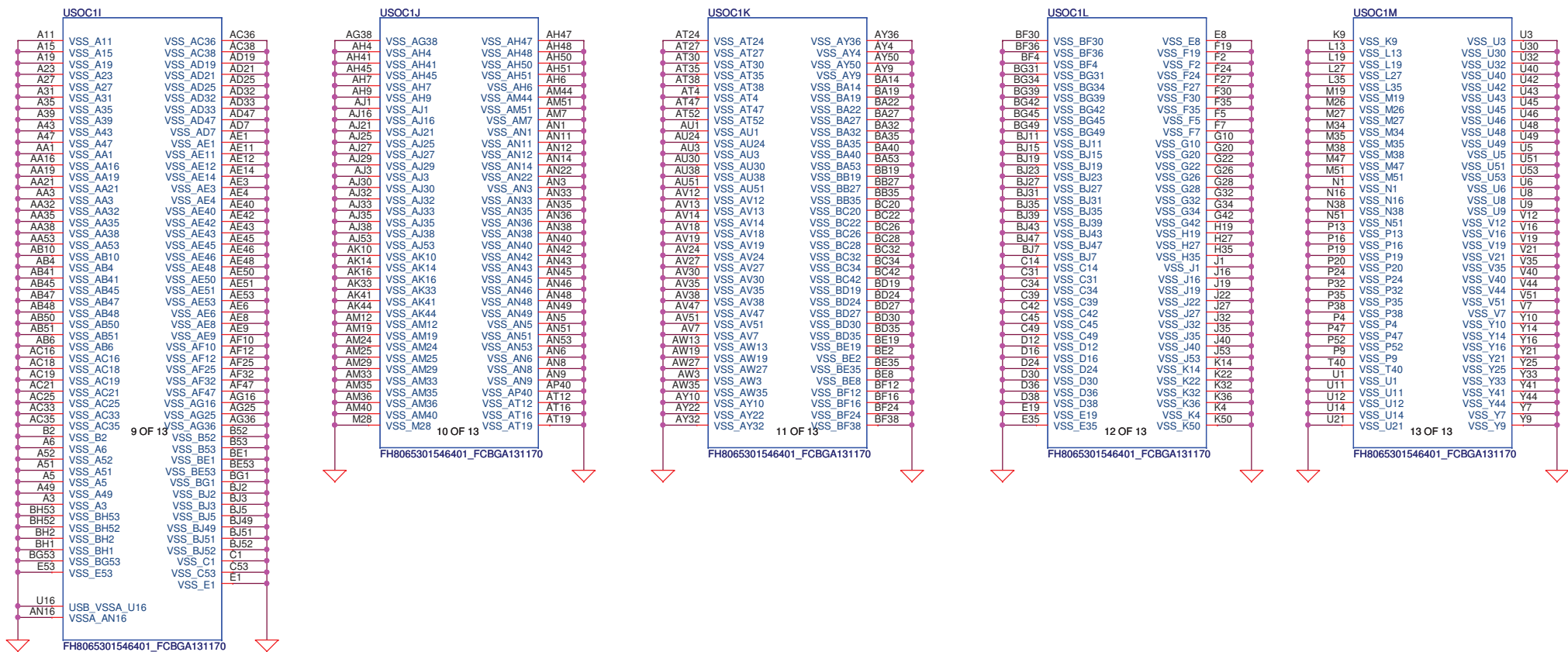




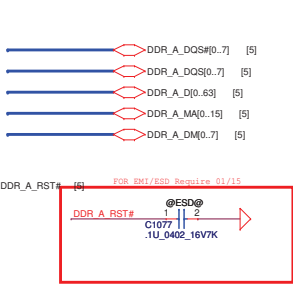
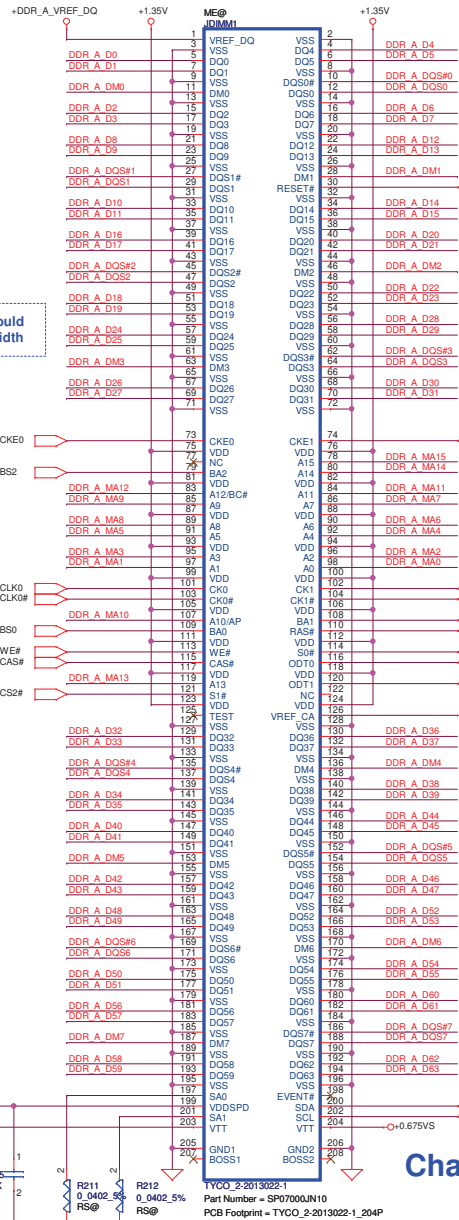




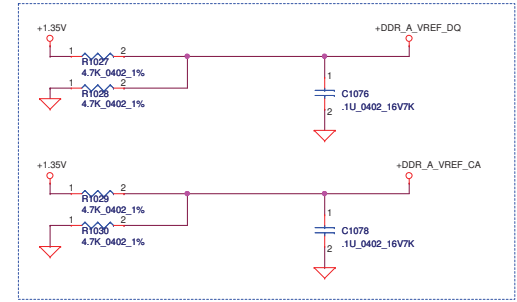
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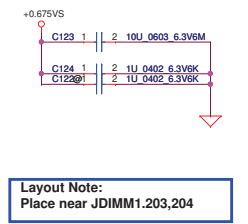
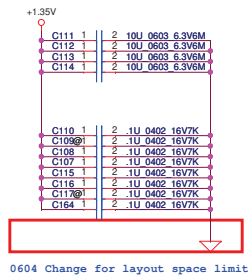


Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO  
DIMMS ON DIMM1\_VREF\_CA / DIMM2\_VREF\_DQ  
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.



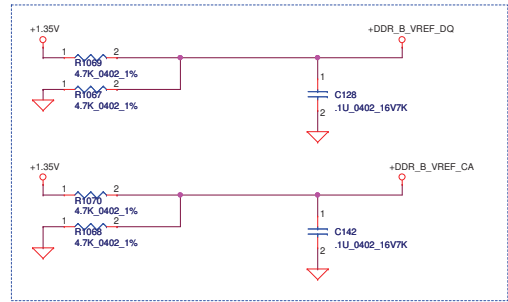
Layout Note:  
Place near JDIMM1

All VREF traces should  
have 10 mil trace width



<Address: SA1:SA0=00 (A0H)>  
**DIMM\_1 STD H:4mm**

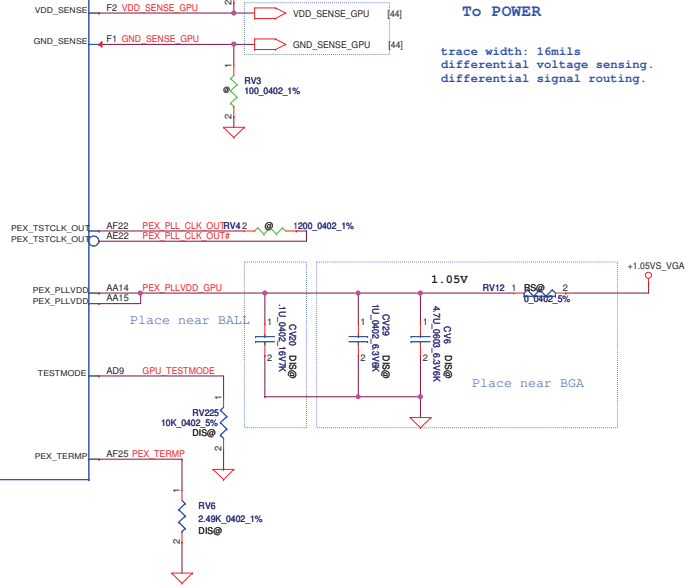
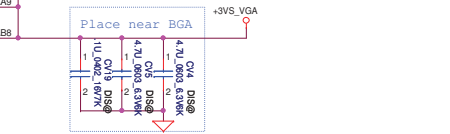
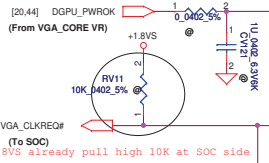
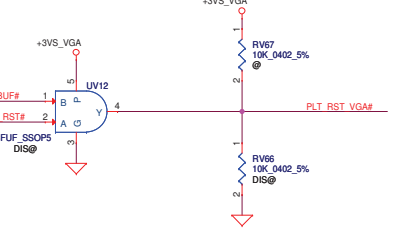
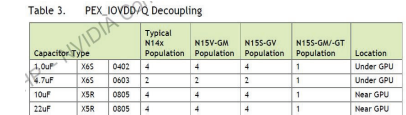
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**<Address: SA0:SA1=10 (A2H)>**  
**DIMM\_2 REV H:4mm**

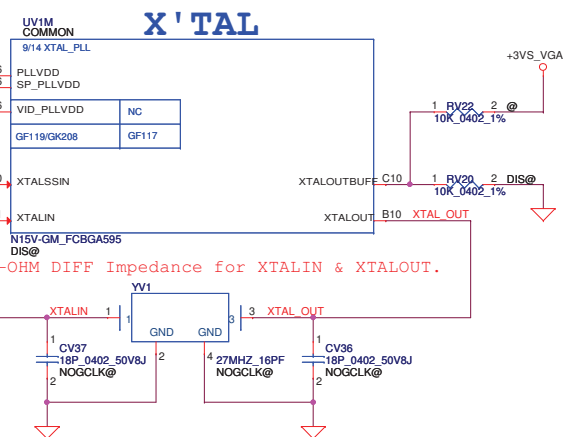
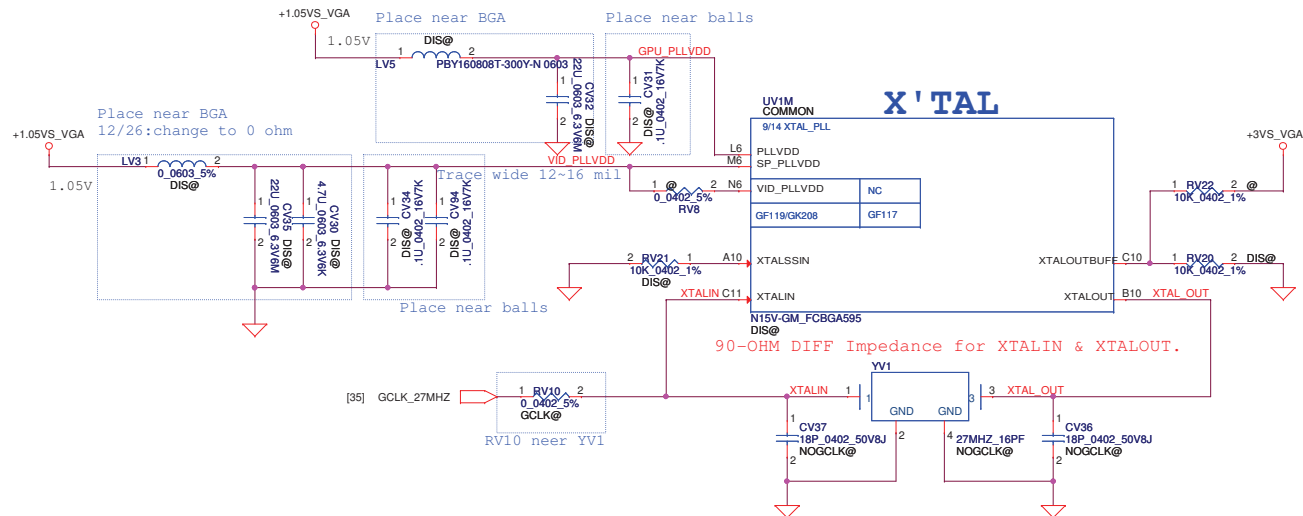
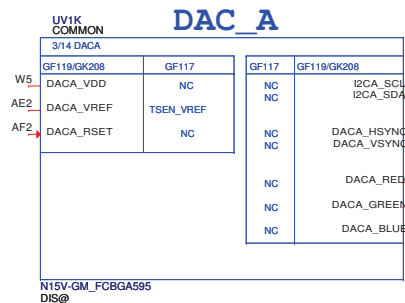
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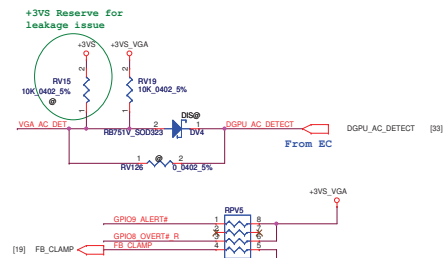
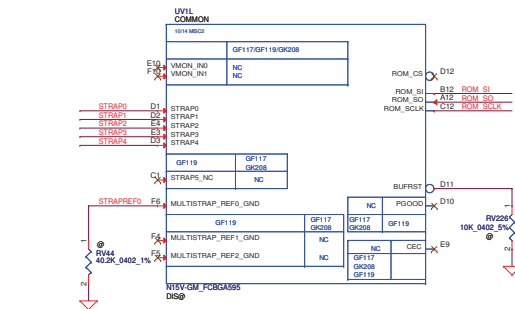
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Link to PCH SML1  
PU @ PCH SIDE

EC\_SMB\_Ok2 [13,14,31,32]

EC\_SMB\_Da2 [13,14,31,32]

The schematic diagram illustrates the VGA output stage. A -3V5\_VGA supply is connected to a network of resistors and capacitors. The resistors are labeled RV90, RV81, RV84, RV83, RV63, RV64, and RV65, all with a value of 10K 0402\_1%. The capacitors are labeled C90, C91, C92, C93, C94, and C95, all with a value of 10K 0402\_1% N15V\_GMP. The output is connected to ROM\_SI, ROM\_SO, and ROM\_SCLK signals.

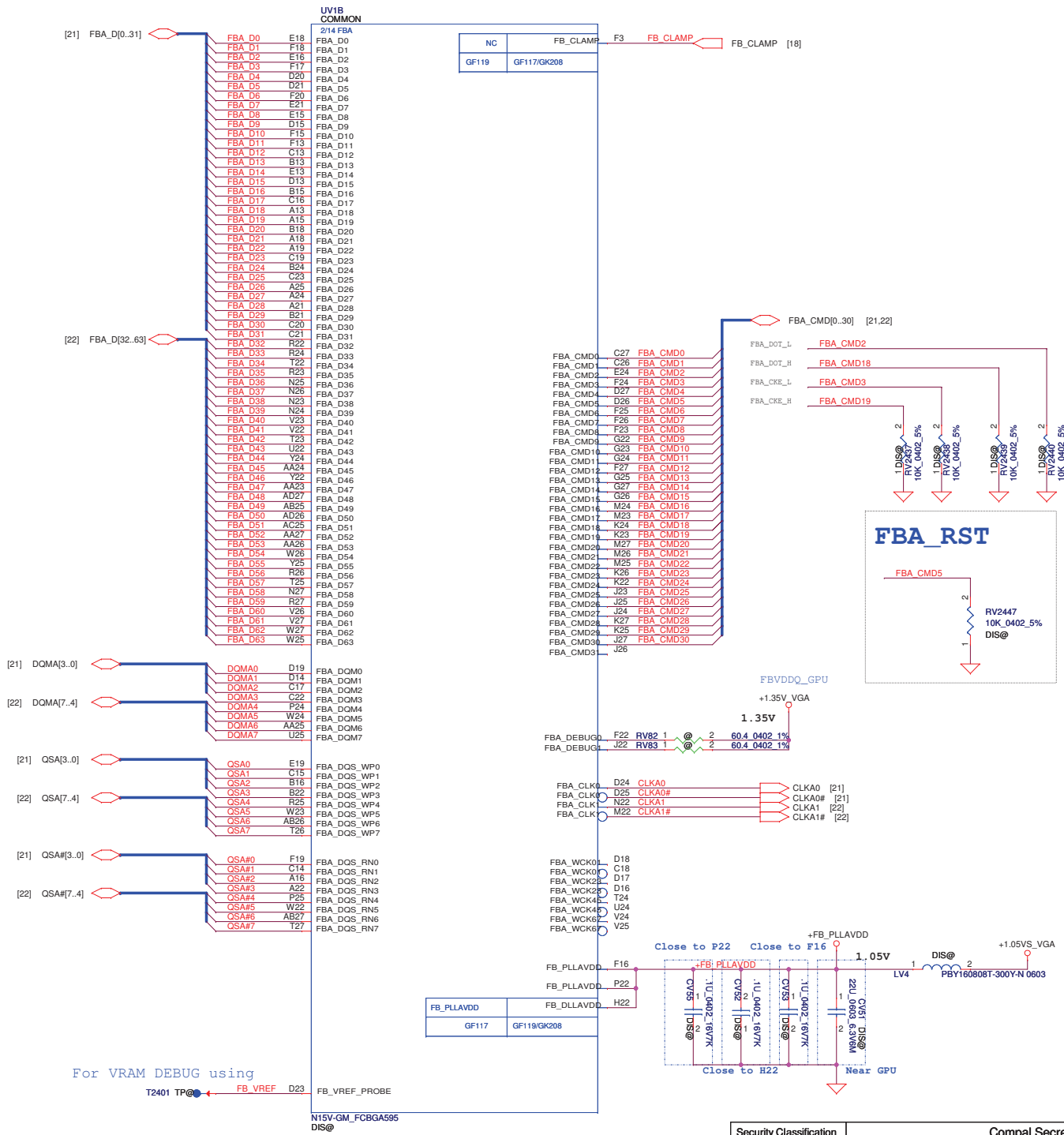
## Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENIDOR	10kΩ	•Pull-up to 3V3 if VBIOS ROM exists •Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)

## Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIF_MAX_SPEED	10kΩ	Pull-down to GND





6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

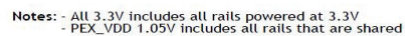
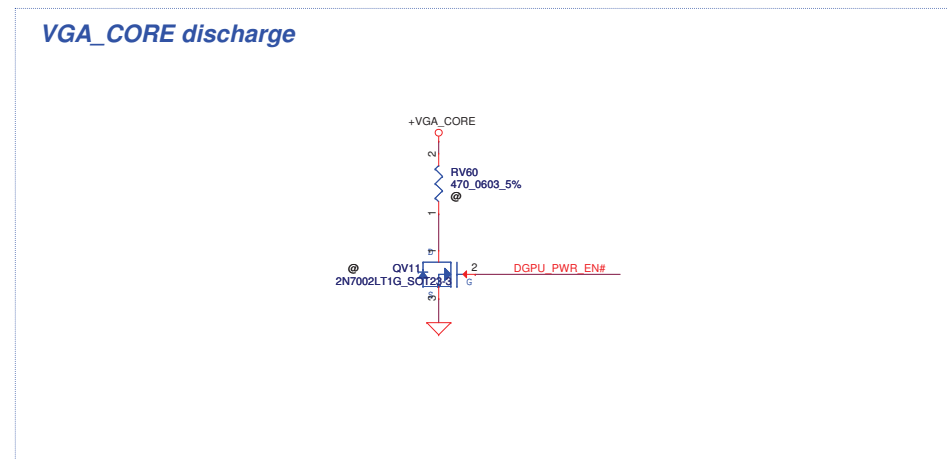
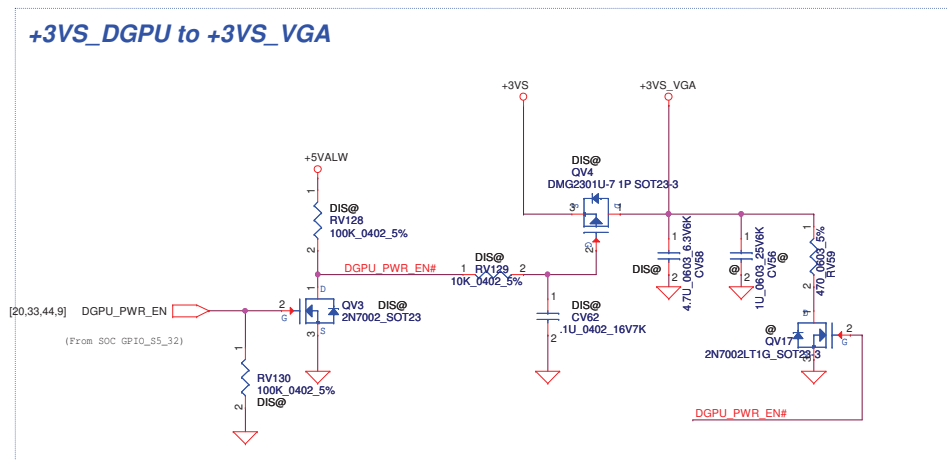


Figure 3-6. Example of Power-up Sequencing Order

**Note:**

- The ramp time for any rail must be more than 40 ns and is recommended to be less than 2ms.



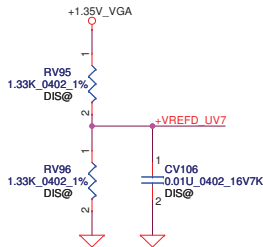
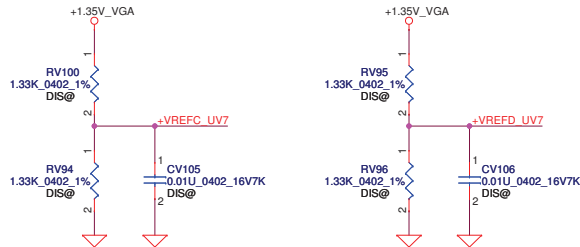
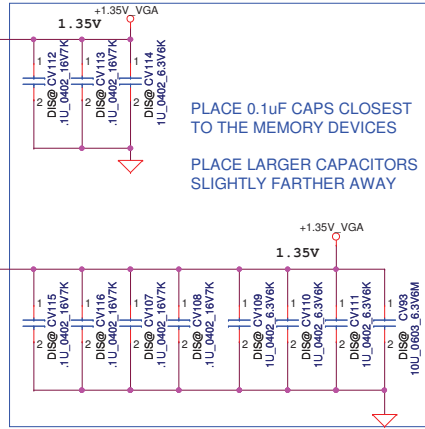
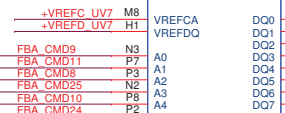
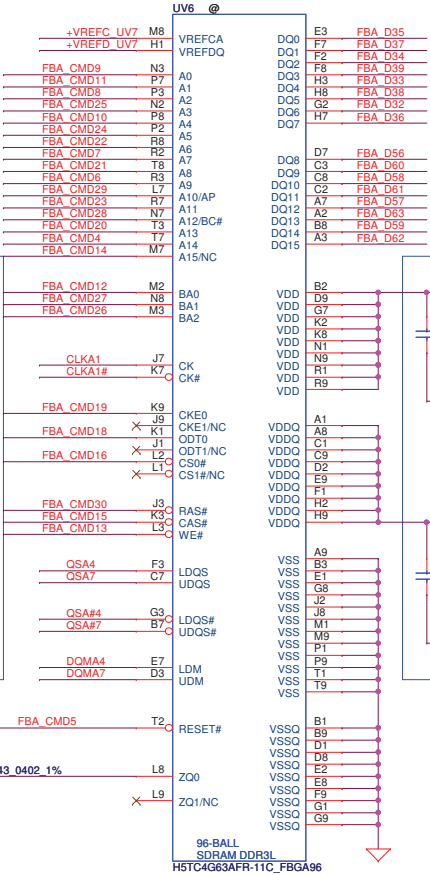
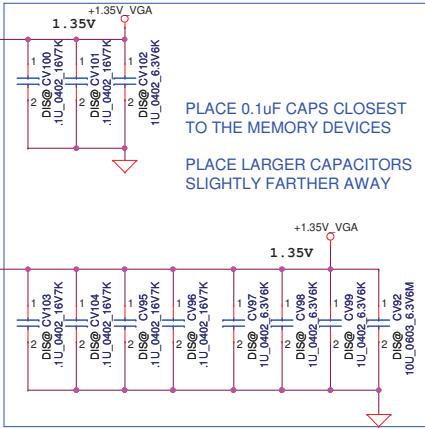
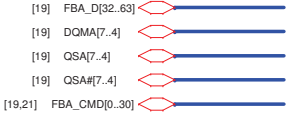
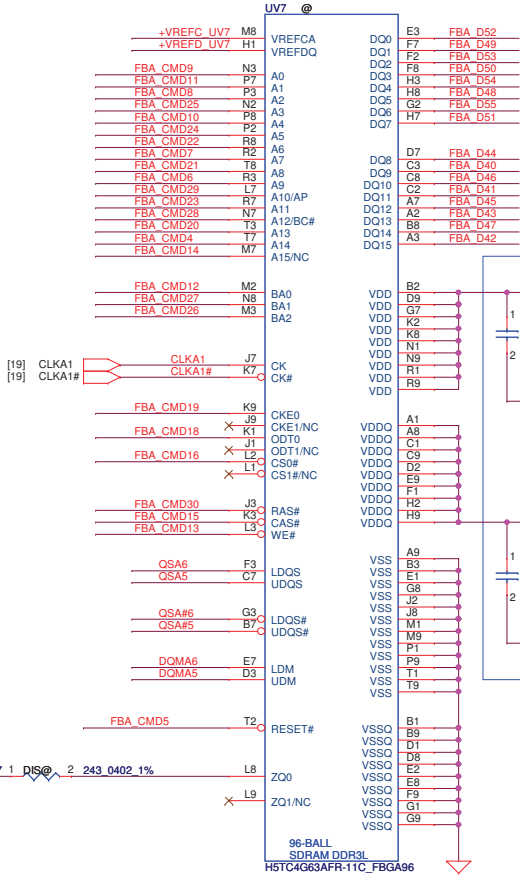
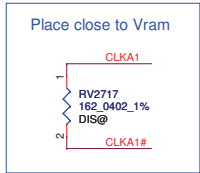
Table 18-1. Optimus Timing Parameters

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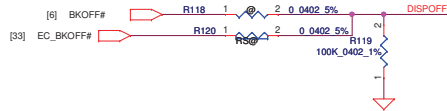
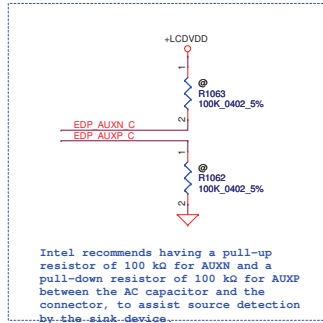
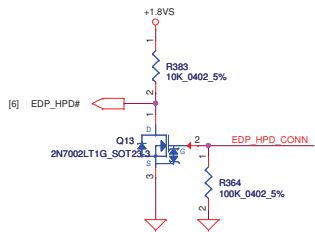
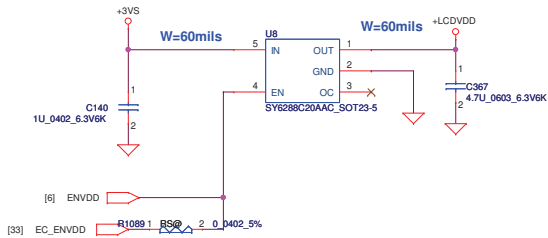
Memory Partition A - Upper 32 bits [64..32]



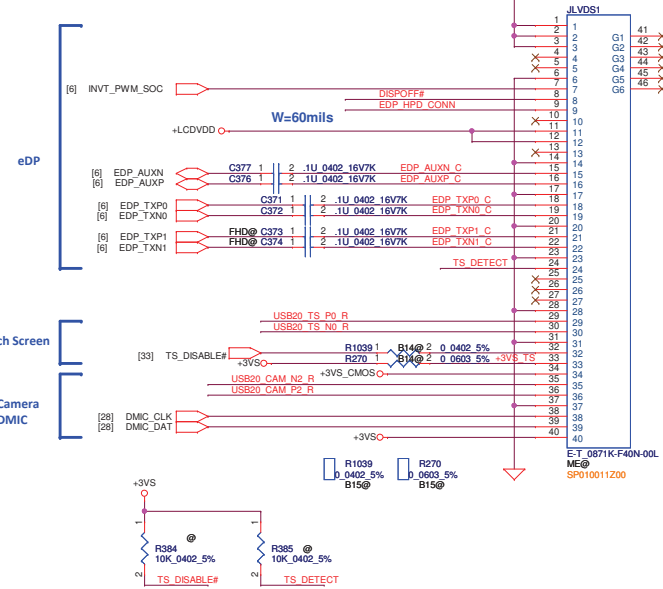
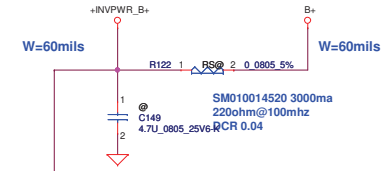
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Date: Tuesday, February 18, 2014				Sheet 22 of 47



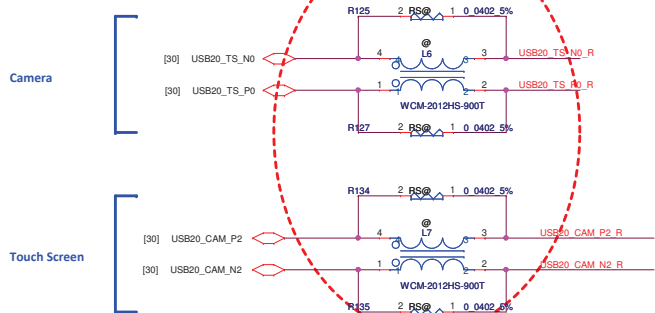
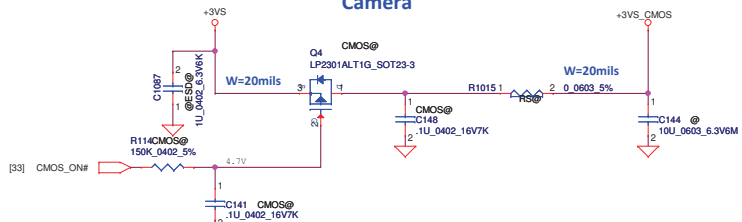
## LCD POWER CIRCUIT



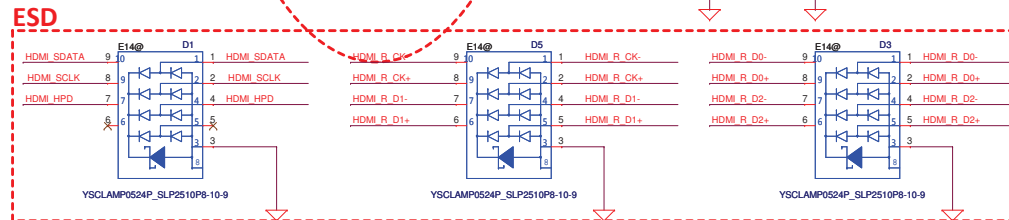
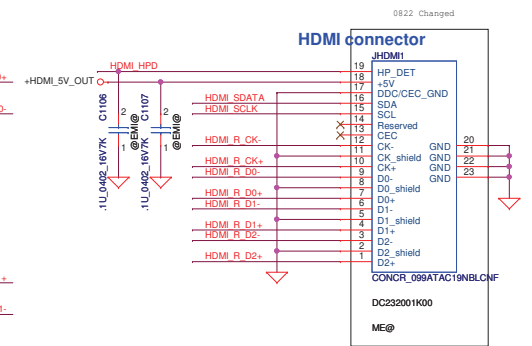
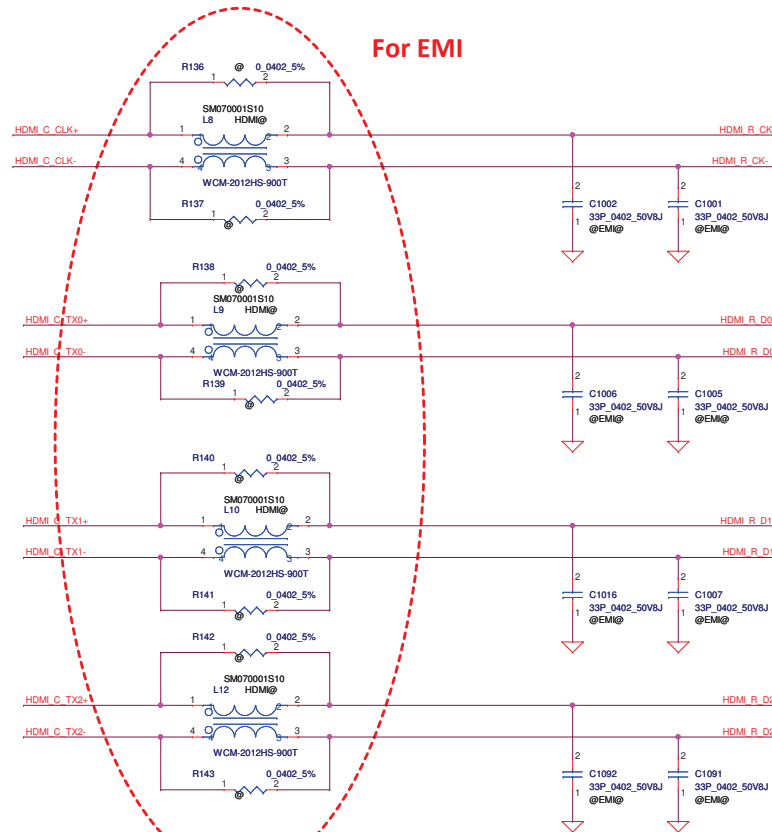
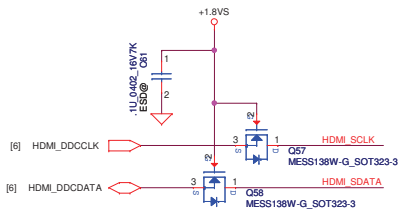
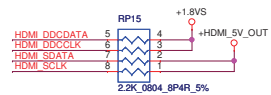
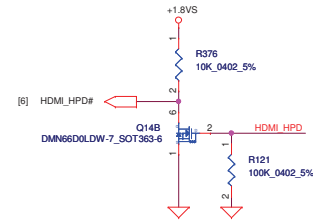
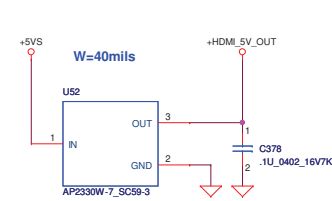
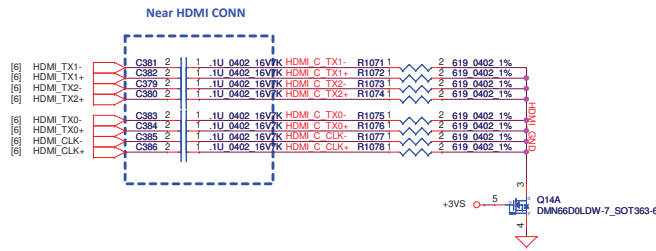
**LCD/ LED PANEL Conn.**



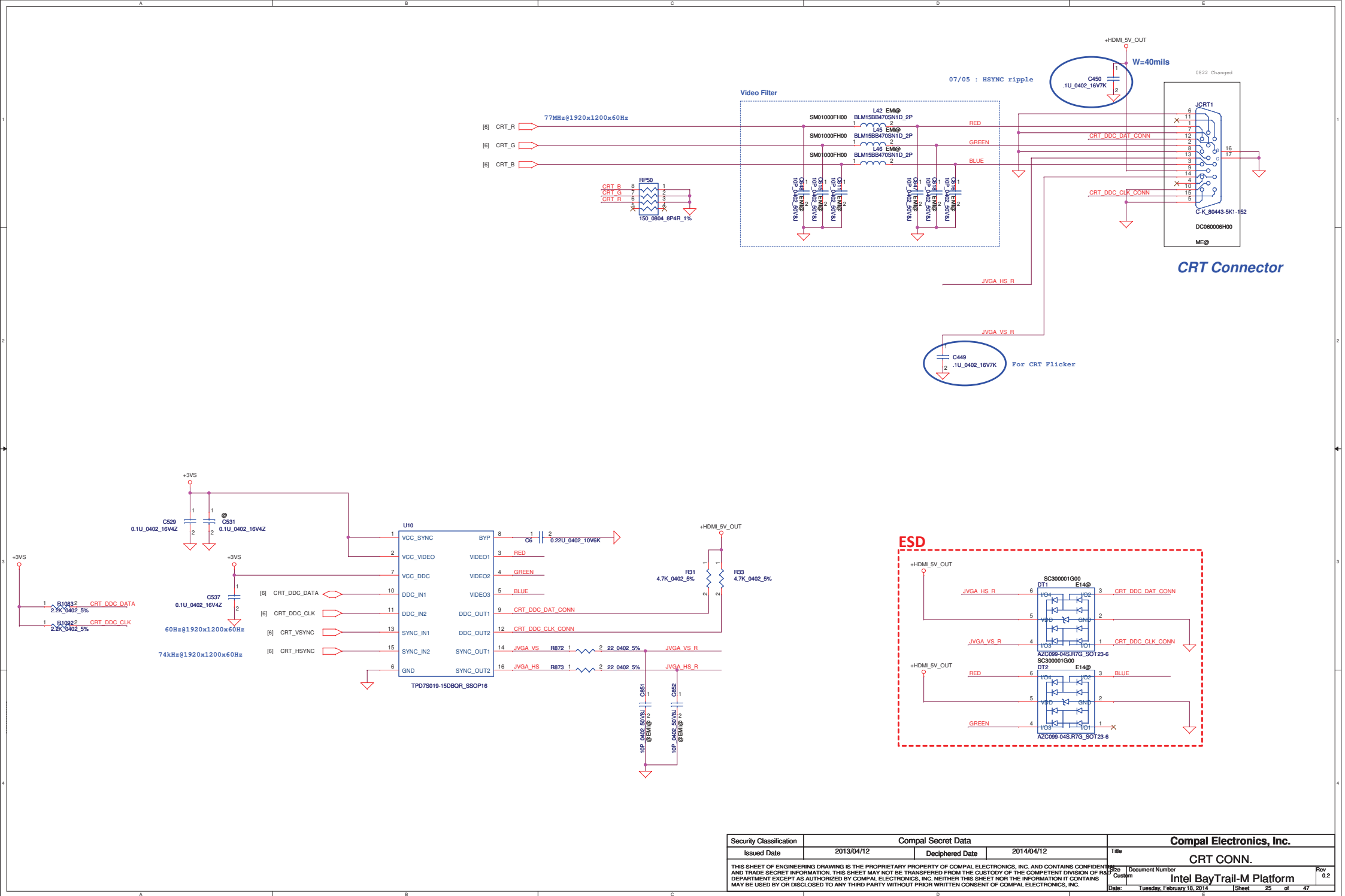
## Camera

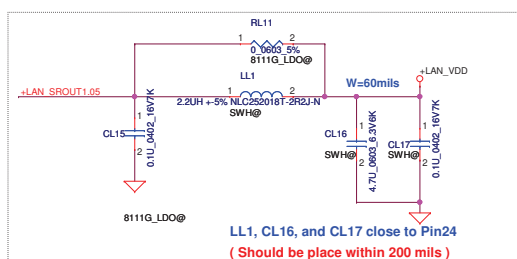
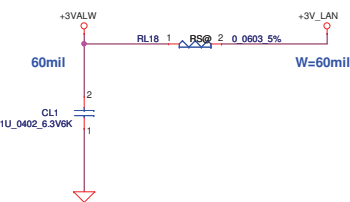


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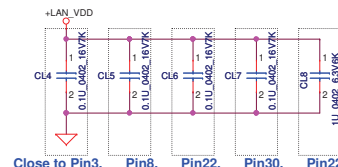
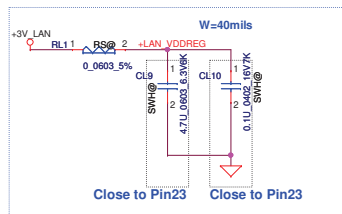
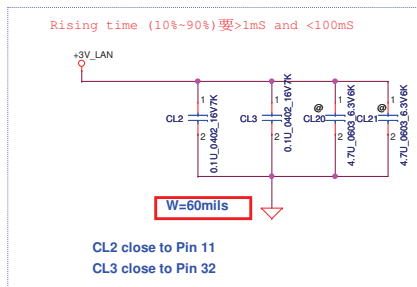
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	HDMI CONN.	
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				Date	Tuesday, February 18, 2014	Rev 0.2
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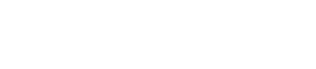
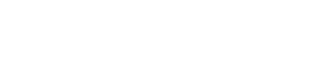
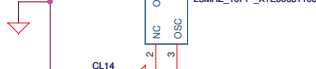
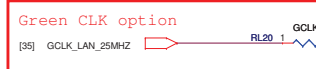
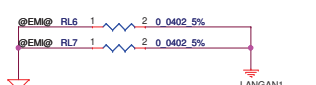
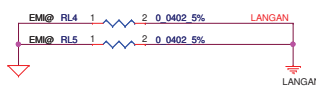
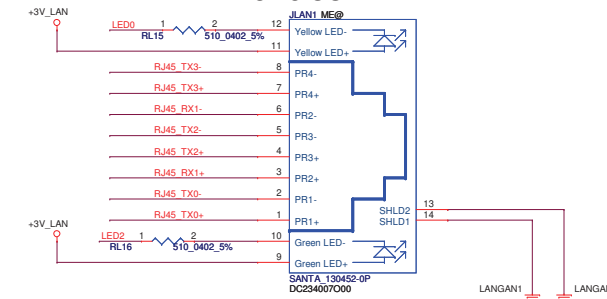


	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005V700	RTL8111G	LDO	X	X	X	O
	RTL8111G	External	X	X	X	O
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X
SA000065Y00	RTL8106E	LDO	X	X	X	X

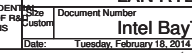
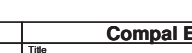
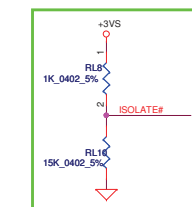
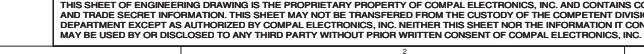
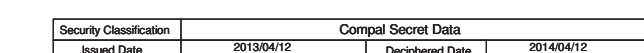
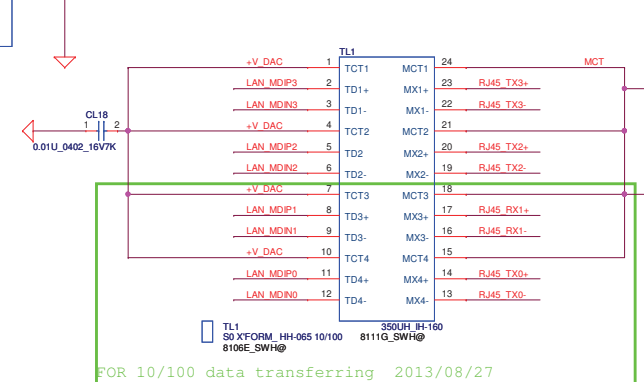
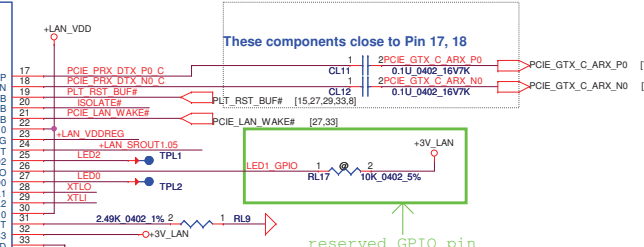
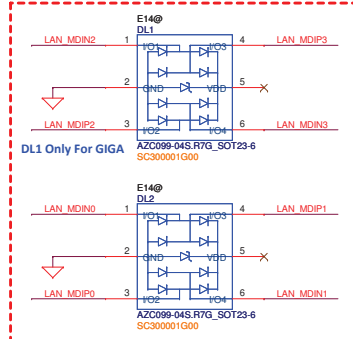
Please refer to the table above when using different 1.0V supply source.  
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.



## RJ-45 CONN.

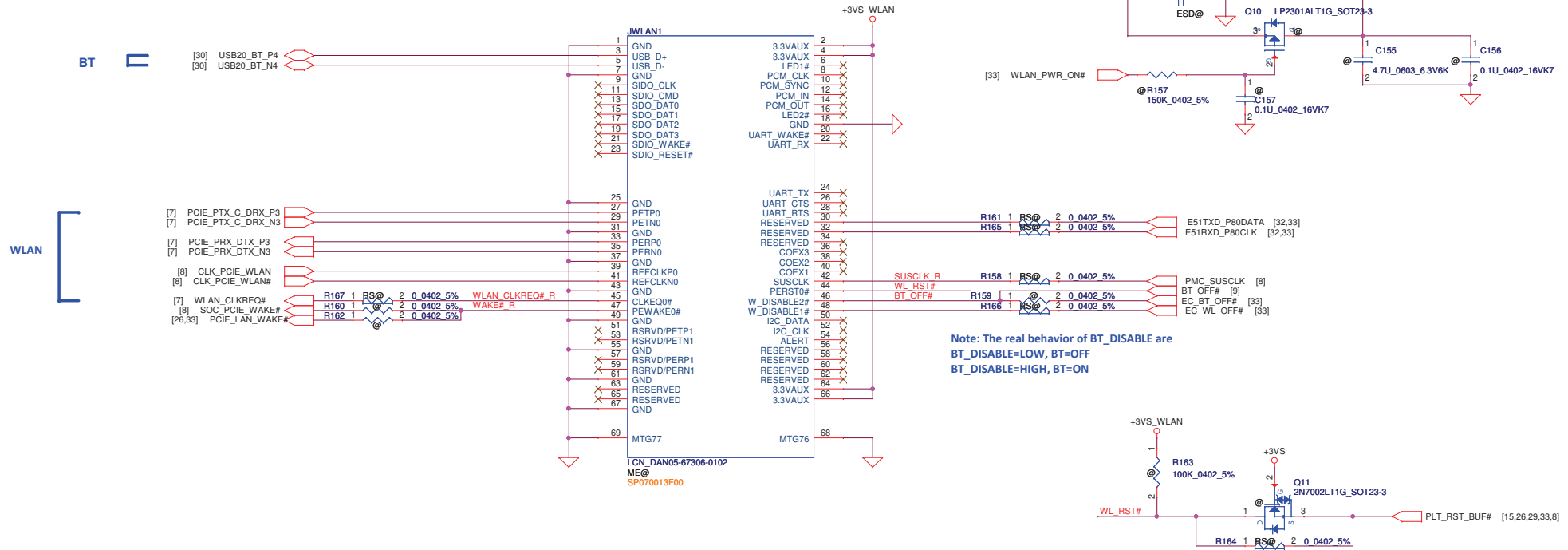


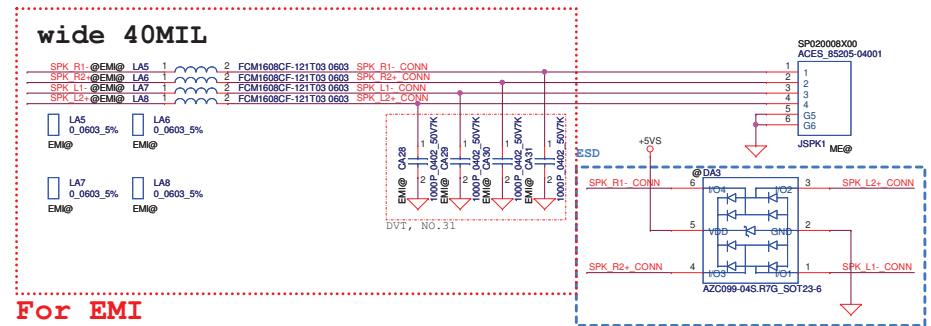
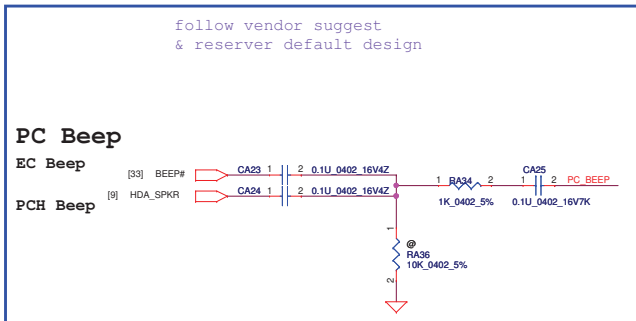
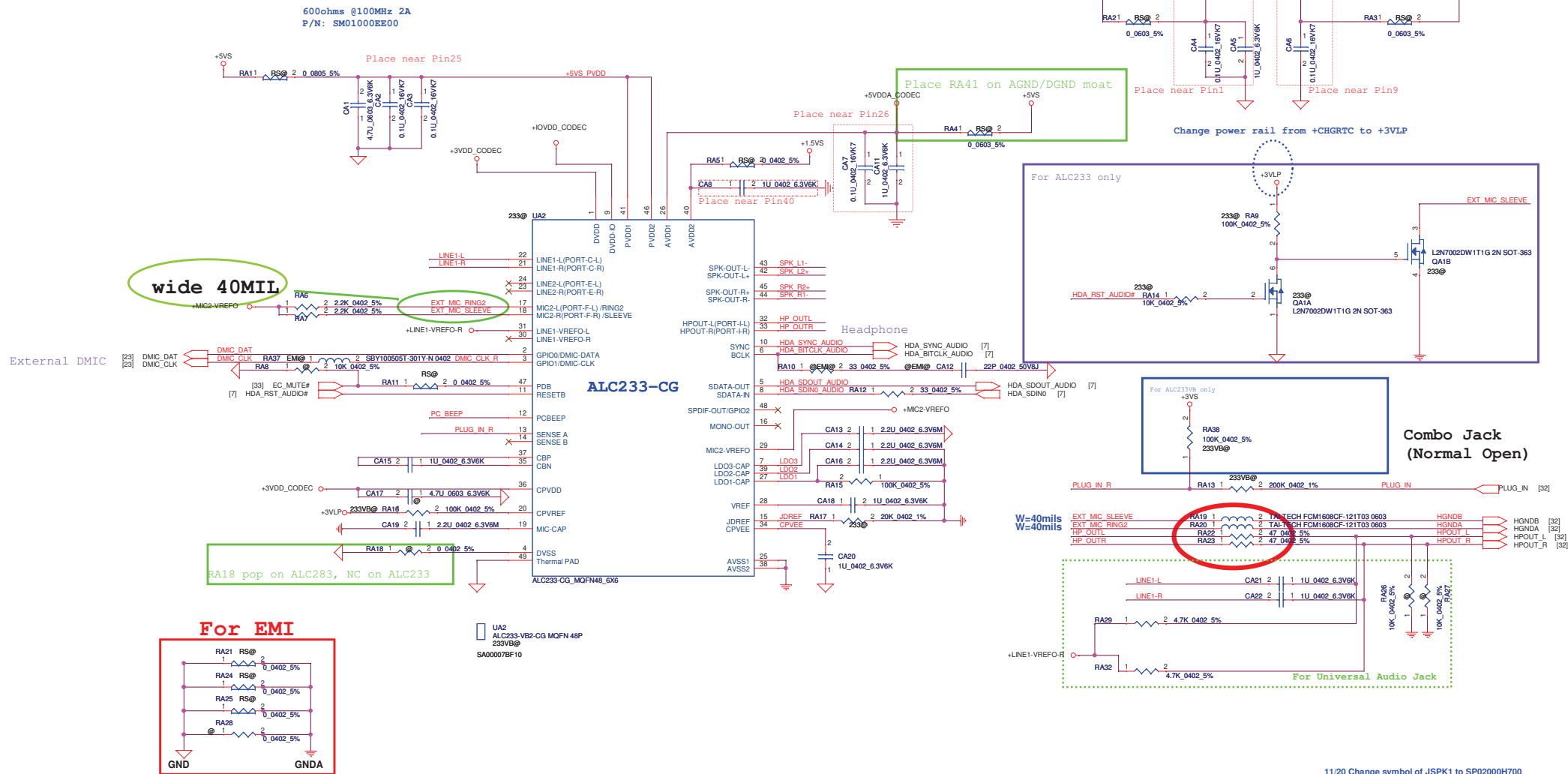
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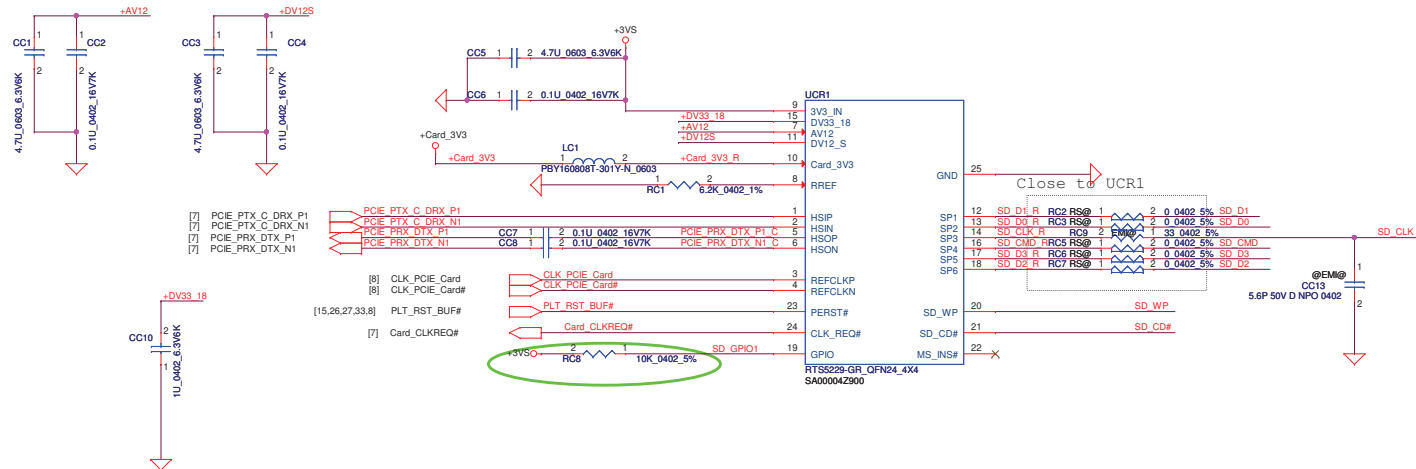
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# NGFF for WLAN / BT(Key E)

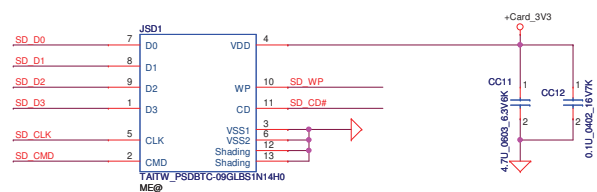




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Date: Tuesday, February 18, 2014				28	47

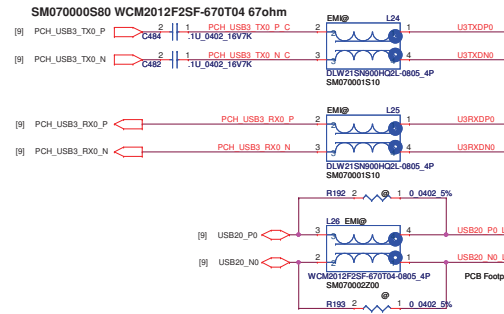
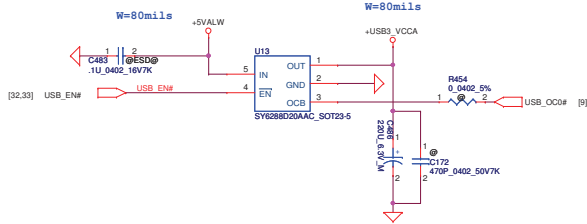


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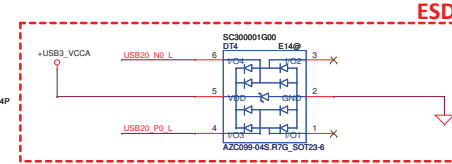
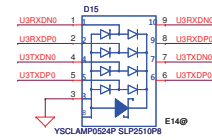


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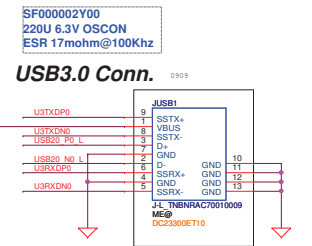




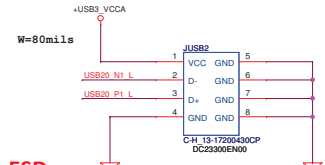
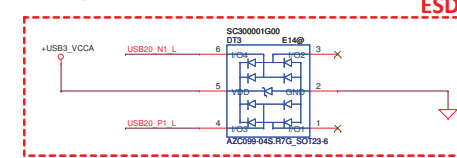
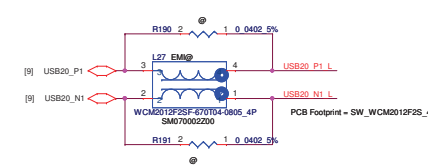
For ESD request



## USB3.0\_Port

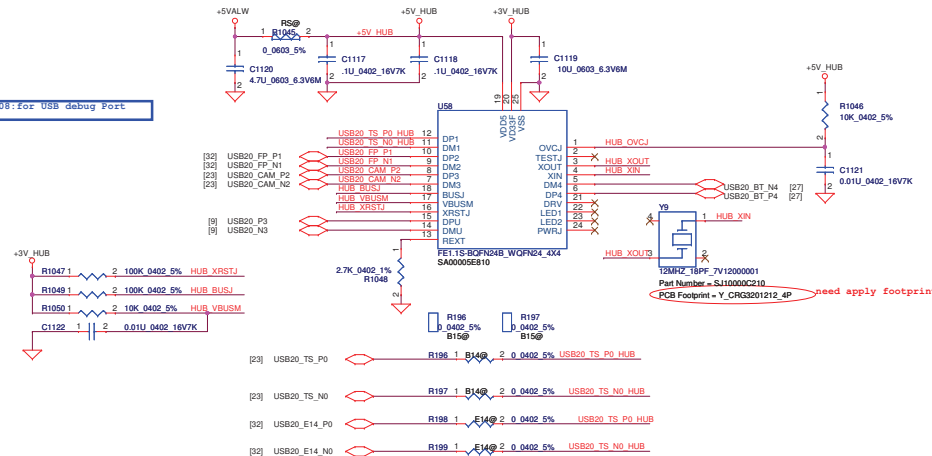


## USB2.0\_Port



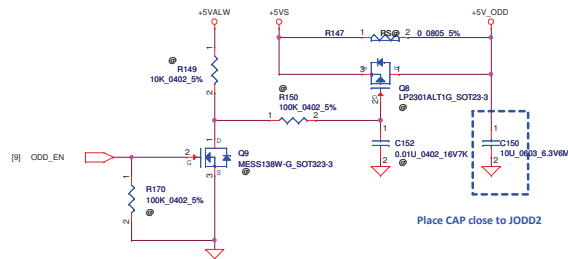
## USB2.0 HUB

0708: for USB debug Port



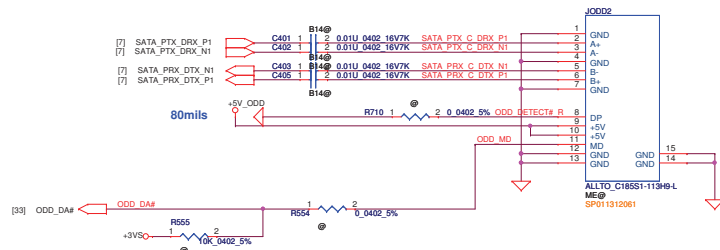
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ODD

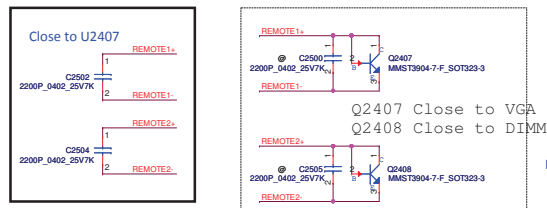
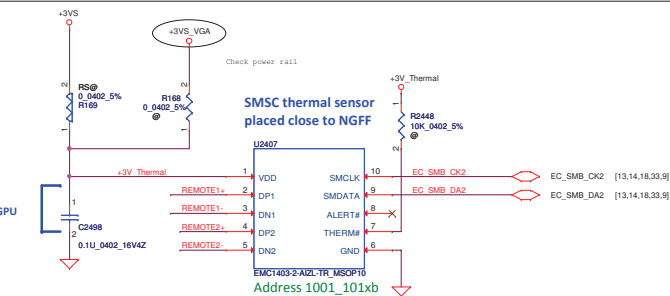
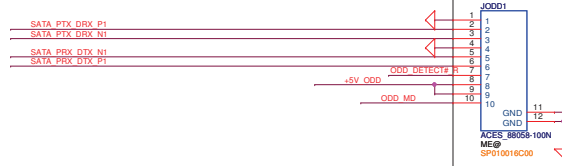


FOR 14"

**SATA ODD Conn.**

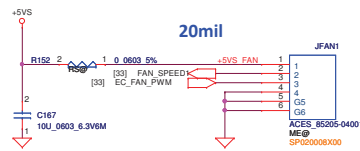


FOR 15" SATA ODD FFC Conn. 0822 changed

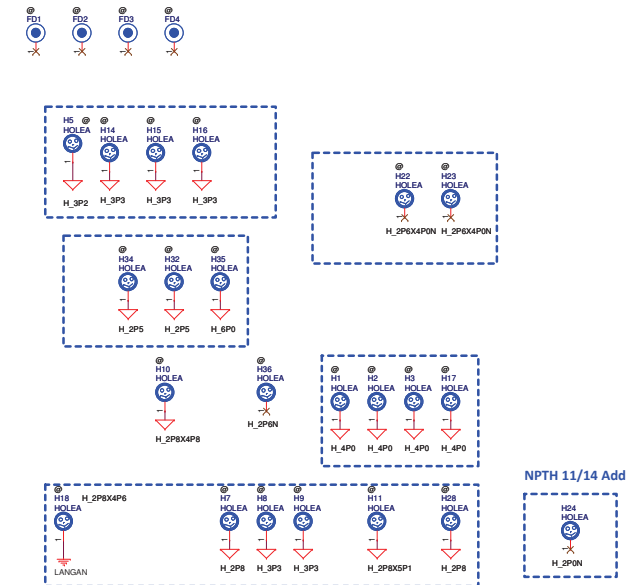
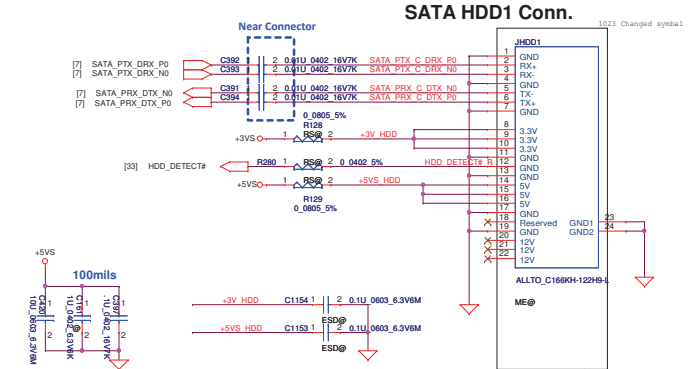
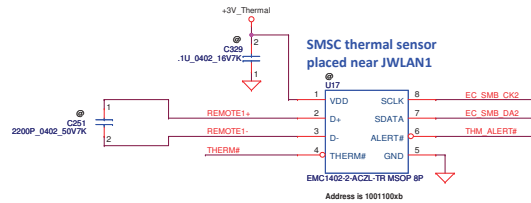


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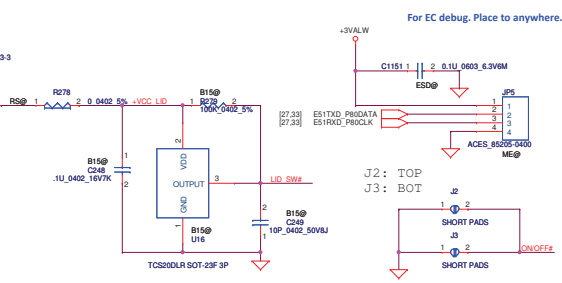
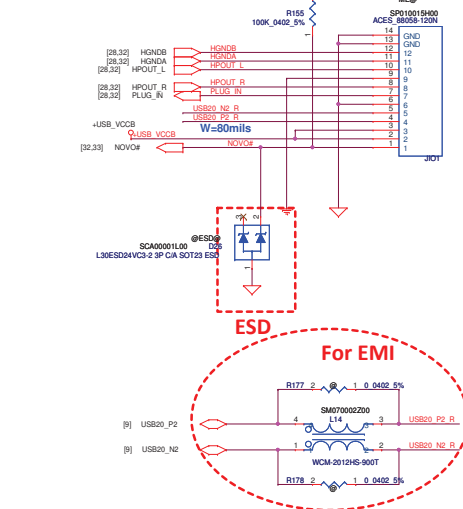
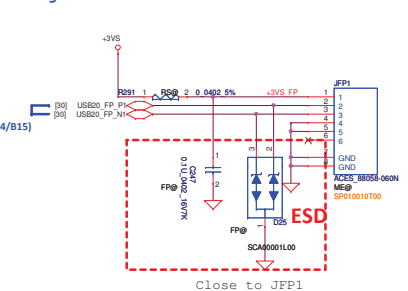
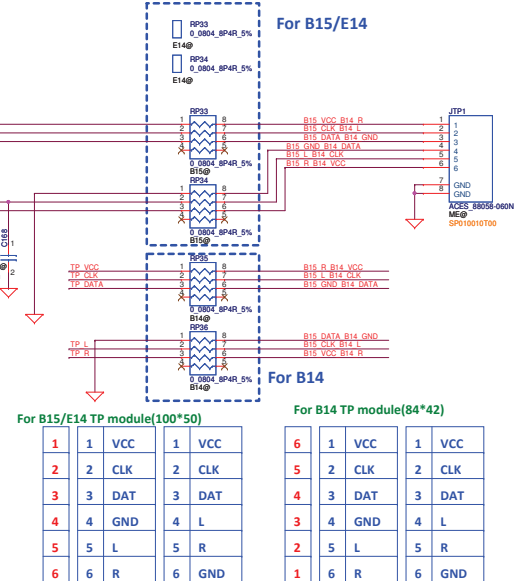
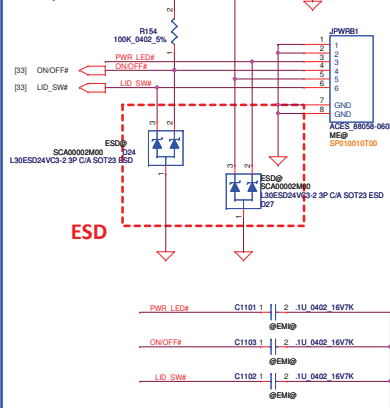
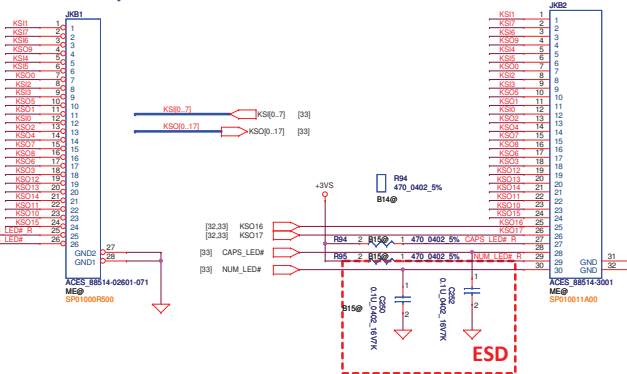
FAN Conn



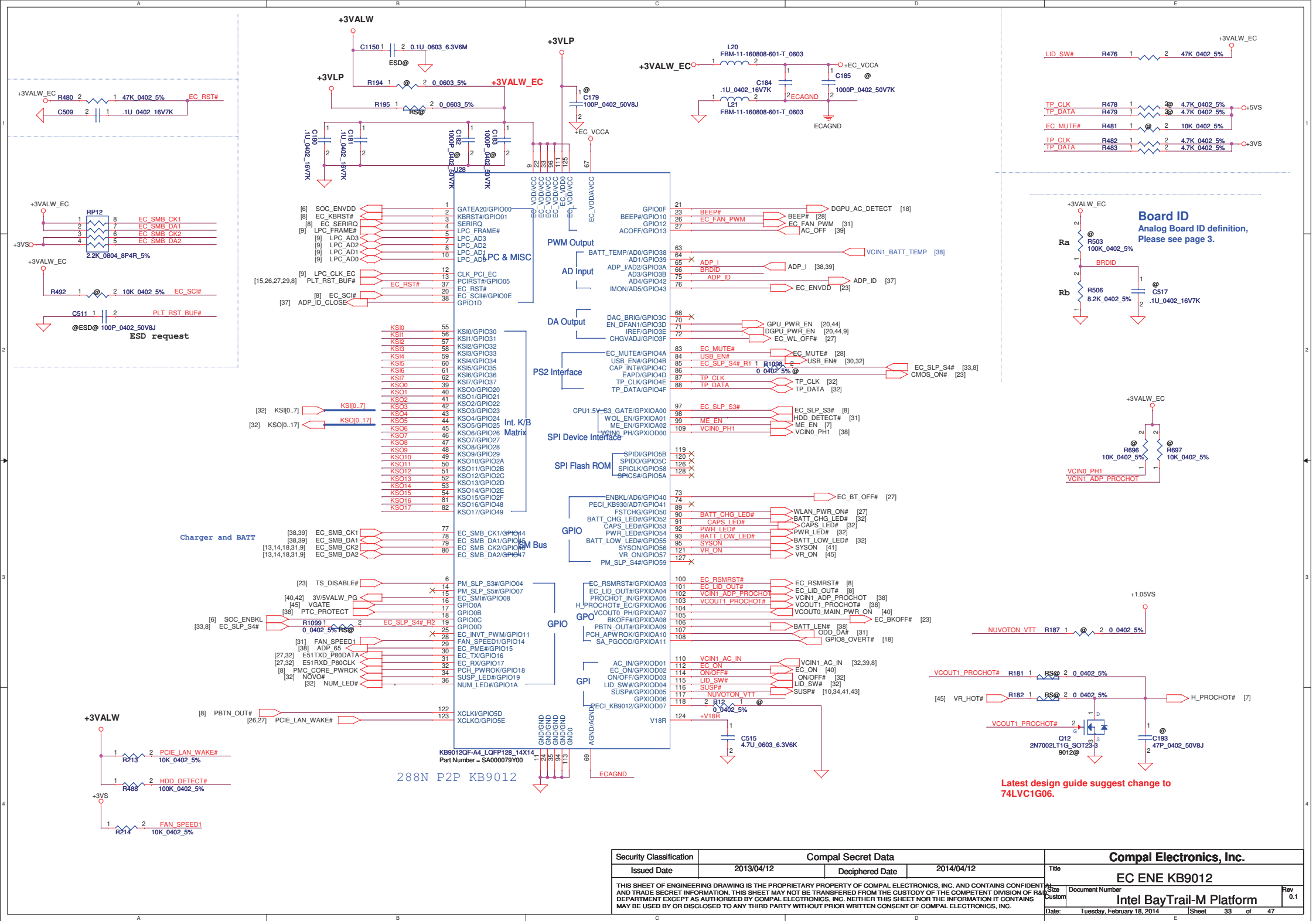
## 2 Channel



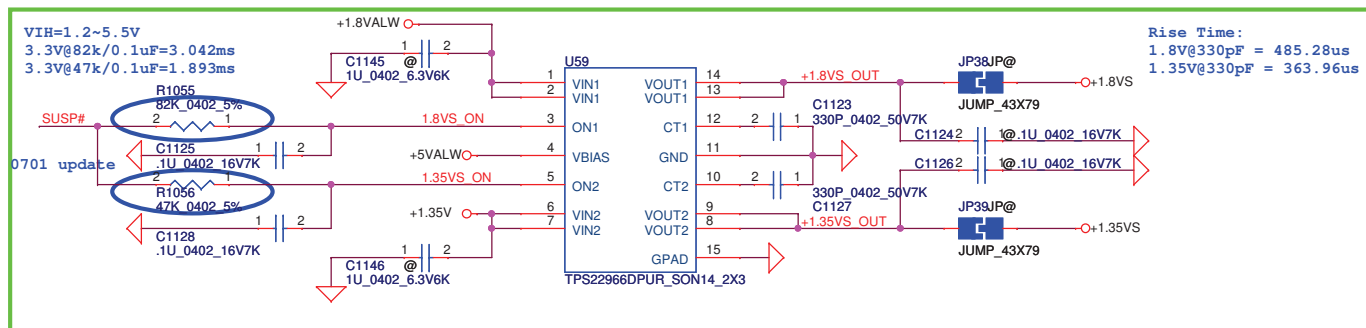
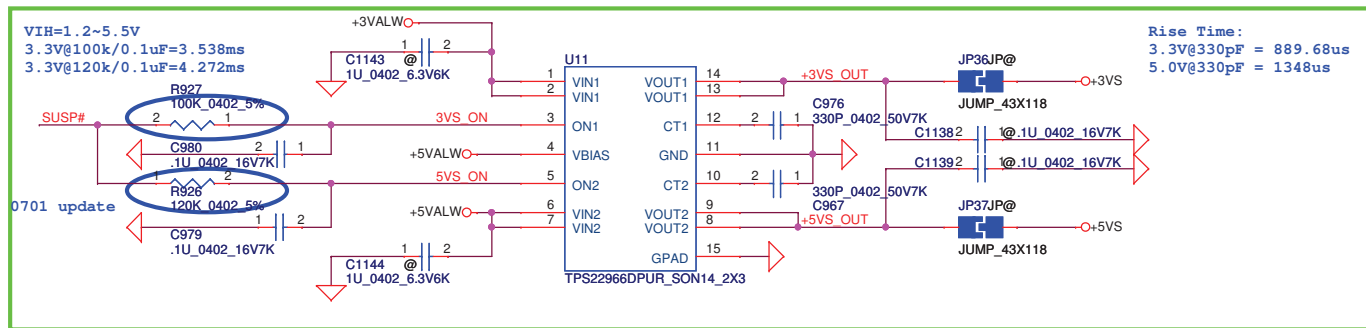
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	HDD/ODD/FAN/Screw Hole	
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Date				Issued	10/19/2014
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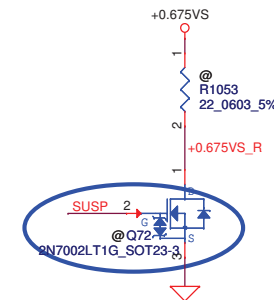
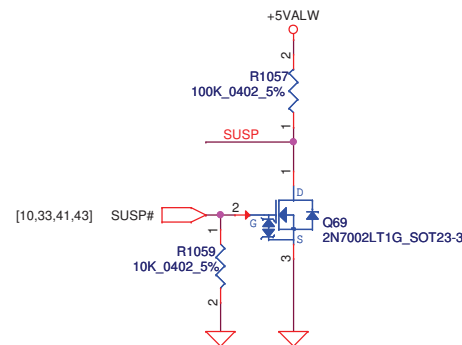
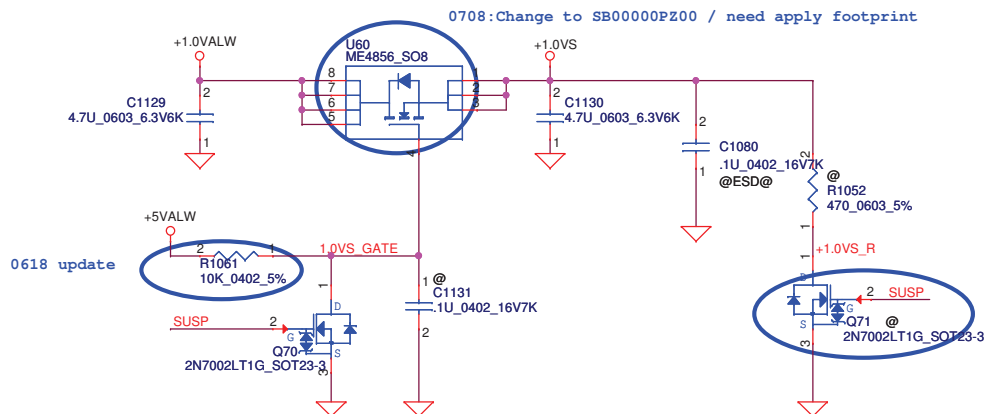
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				Custom	Intel BayTrail-M Platform	0.1			
				Date:	Tuesday, February 18, 2014	Sheet	33	of	47



## +1.0VALW TO +1.0VS



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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	DC INTERFACE
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				Document Number	Intel BayTrail-M Platform
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For UMA

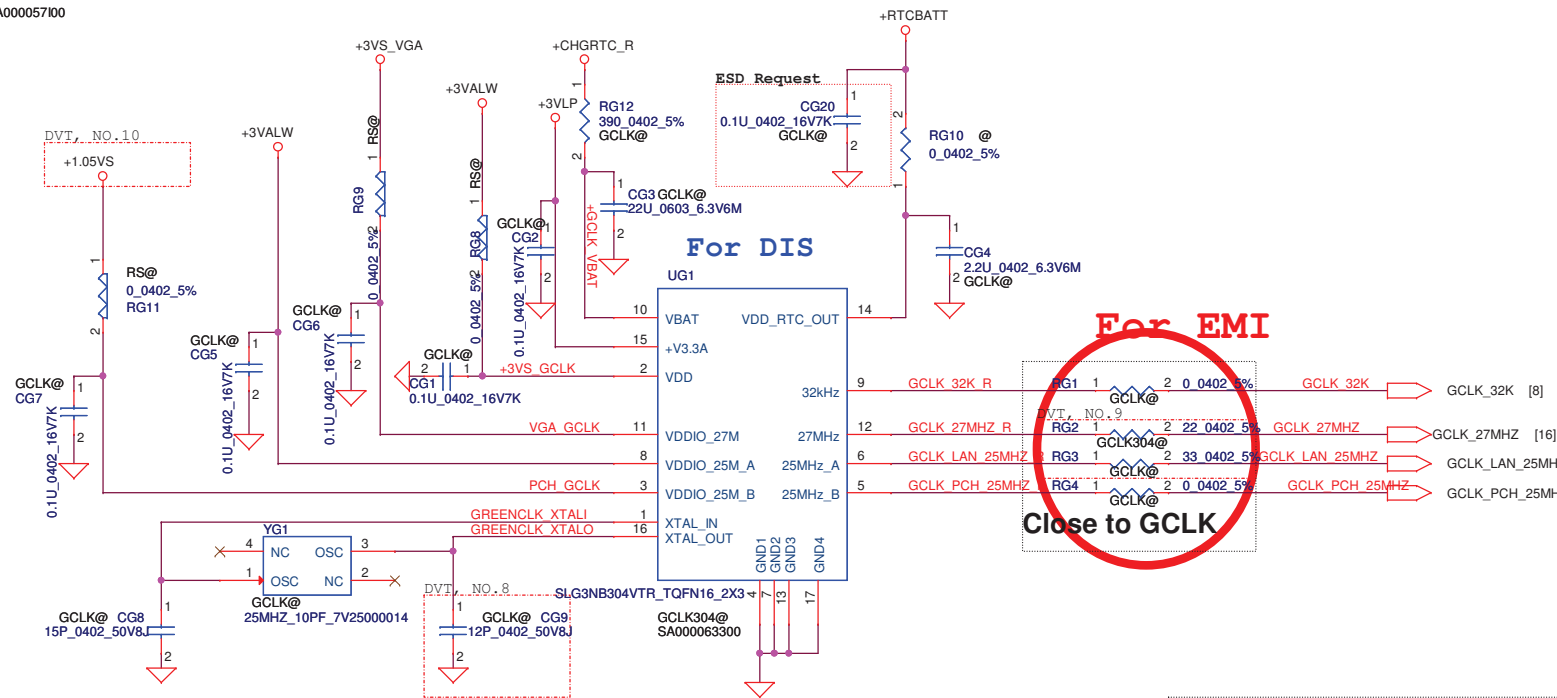
UG1 GCLK244@



SLG3NB244VTR\_TQFN16\_2X3

SA000057100

Every power trace need:  
W=20mils

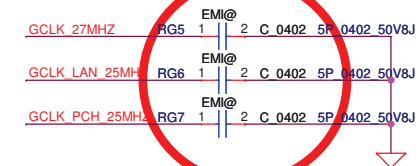


For EMI

Close to GCLK

SOC\_32.768K  
NV\_VGA  
LAN  
SOC\_25M

Reserved for Swing Level adjustment  
( Close GCLK side )



For EMI

Security Classification		Compal Secret Data		Title	
Issued Date	2012/10/11	Deciphered Date	2014/10/11	P35-GCLK	
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## Page 1 of 1 for HW PIR

Item	Reason for change	PG#	Modify List	Rework verify	Phase
1	Add Net "EC_SLP_S4#_R1" and "EC_SLP_S4#_R2 by vendor suggestion	33	Add R1098,R1099	V	SIV
2	Reduce component count,delete 12 pcs resister and add 4 pcs row resister.	32	Delete R311,R312,R313,R265,R266,R298,R316,R315, R314,R302,R303,R304, Add RP33,RP34,RP35,RP36	V	SIV
3	Audio vendor suggestion	28	Change CA16,CA13,CA19,CA14 from 0603 to 0402 Change CA11 from 4.7u to 1u , unpop CA17.	V	SIV
4	Nuvoton suggestion to add resister at PIN118 to GND	33	Add R12	V	SIV
5	ESD Team solution		Add C60,C61,C62,C514,C516,C518,C519,C520,D27(reserve)	V	SIV
6	HW strap pin	8	Add R1100,R1101,R1102,R1103,R1104,R1105	V	SIV
7	VGA sequence tuning	20	Add RV23	V	SIV
8	EMI solution	28 & 29	Change RC9 from 0 ohm to 33 ohm POP CA28,CA29,CA30,CA31	V	SIV
9	ESD solution		Add C1080,C1081,C1082,C1083,C1084,C1085,C1086,C1087,C1088	V	SIV
10	EMI solution for DDR DIMM	10	Reserve C1189,C1190,L51,L52	V	SIV
11	ESD request to delete XDP test point	8	Delete T198,T199,T200,T209,T210,T211,T212	V	SIV
12	EMI request	10	Change R1017 from shortPAD to 0 ohm	V	SIV
13	Delete 0 ohm due to 15'' ODD can short direct	31	Delete R130,R131,R132,R133	V	SIV
14	ME request	31	Modify H35 footprint to H_6P0,H8 & H9 to H_3P3		SIT
15	ME request	31	Change JODD2 P/N from SP01001RS00 to SP011312061		SIT
16	Protect EC	23	JLVDS1 pin 6 pull down	V	SIT
17	Vendor request	33	Modify U11.111 connect to +3VLP only,C179.1 connect to +3VLP	V	SIT
18	Vendor suggestion	20	+1.05VS to +1.05VS_VGA power switch enable pin reserve DGPU_PWR_EN path	V	SIT
19	Sourcer suggestion	31	Change Q2407,Q2408 P/N from SB000008E00 to SB000002R00	V	SIT
20	EMI request		Reserve C1001,C1002,C1005,C1006,C1007,C1016,C1091,C1092,C1101, C1102,C1103,C1104,C1105,C1106,C1107	V	SIT
21	ESD request		Add C1149,C1150,C1151,C1152,C1153,C1154	V	SIT
		Security Classification		Compal Secret Data	
		Issued Date		Deciphered Date	
		2013/04/12		2014/04/12	
		Title		Intel BayTrail-M Platform	
		Document Number		Rev 0.2	
		Date:		Tuesday, February 18, 2014	
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